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(54) Title of Invention: Production Method of Packaging for Semiconductor Equipment

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Detailed Descriptions:

1. Title of Invention:

Production Method of Packaging for Semiconductor Equipment

2. Scope of Patent Claims:

The production method of packaging for semiconductor equipment, which is characterized as being equipped with semiconductor equipment on the substrate that is composed of such a material that is possible for a selective etching, tying up the connecting wire with the above-mentioned semiconductor equipment as well as putting together the external electrode parts of the connecting wire with the extreme end of the external electrode parts of the above-mentioned substrate, and resin molding all together the above-mentioned connecting wires on the above-mentioned substrate, as well as removing etching from the above-mentioned substrate in the last stage.

3. Detailed Descriptions of Invention:

Areas of Industrial Applications:

This invention is in regard to the production method of packaging for semiconductor

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equipment.

The background technologies and their problems:

Conventionally, the so-called chip-carrier type packaging has been used widely as one of the methods for producing packaging on the printed substrate with high accuracy. This method is of a lead-less type packaging method, through which an electrode, which is being extended to the rear surface of the packaging, is connected directly to the conductor pattern on the printed substrate by soldering.

There are two (2) types of methods in this chip-carrier type packaging, namely, a ceramic type method and plastic type method. However, not only that the packaging made by the ceramic type method is expensive, but also it has such a disadvantage that a cracking and/or peeling might occur at the connections between the ceramics and above-mentioned soldering parts and/or the conductors, due to the

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differences of their coefficient of thermal expansion during the temperature cycle, when soldered directly to the printed substrate. On the other hand, however, although the packaging by the plastic type method is less expensive, it also has such disadvantages that a heat dissipation capacity is being poor, as well as the shape itself is not suitable for the automation of the packaging.

In Fig. 1, the construction of this conventional plastic type chip-carrier packaging is shown. This packaging (1) is produced in such a way that by dropping a liquid epoxy resin from the above, onto the parts, after having connected both ends of the chip (4) and electrode (2) through a wire bonding method with small size wires (5) of Au, after setting the chip (4), which is

consisting of the semiconductor equipment, onto the printed substrate (3), on which the electrode (2) of copper film is being formed in advance.

At this packaging (1), the resin layer (6) and printed substrate (3) surround the chip (4). Since the heat resistance of these resin layer (6) and printed substrate (3) is relatively higher, the heat that is generated by the chip (4) while it is working cannot be removed effectively towards outside of the packaging (1). That is to say that, the heat dissipation characteristic of the packaging (1) is poor, and it is one of the disadvantages of this particular component. Moreover, when the liquid resin epoxy is dropped onto the parts from above, as mentioned previously, it is pretty difficult to control the small specific amount of liquid dropping at a higher speed with a constant manner, thus making it very difficult to handle the packaging (1) with an automated mode.

On the other hand, there is a packaging that is called as a tape-carrier type packaging, which is different from the chip-carrier type packaging. Compared with the conventional type of chip-carrier type packaging, this type of packaging has such an advantage that the unit can be made much smaller. However, it also has some other disadvantages as such that, the heat dissipation characteristic is poor, as the chip is totally covered by the resin layer, as well as it requires a special equipment as being employed with a tape.

The Objective of the Invention:

The objective of this invention is that, to provide a production method of packaging for semiconductor equipment, which has a high heat dissipation capacity as well as with more reliable capabilities, so that the above-mentioned conventional problems can possibly be solved.

The Outline of the Invention:

The production method of packaging for semiconductor equipment, which is related to this

invention is characterized as being equipped with semiconductor equipment on the substrate that is composed of such a material that is possible for a selective etching, tying up the connecting wire with the above-mentioned semiconductor equipment, as well as putting together the external electrode parts of the connecting wires with the extreme end of the external electrode parts of the above-mentioned substrate, and resin molding all together with the above-mentioned connecting wires on the above-mentioned substrate, as well as removing etching from the above-mentioned substrate in the last stage. By doing it this way, it is possible that to produce the lead-less type packaging for semiconductor equipment, which has a high heat dissipation capacity as well as with more reliable capabilities, through an automated, simple, and less expensive way. The external electrode parts, which are mentioned above may be represented by the above-mentioned connecting wires, and/or may be separated from the above-mentioned connecting wires, and be connected to the above-mentioned connecting wires.

Implemented Examples:

In the following, the production method of packaging for semiconductor equipment, which is related to this invention is described by using some sketched diagrams based on the implemented examples.

Fig. 2A ~ 2D are showing the process diagrams to explain the production method of packaging for semiconductor equipment, which is related to this invention by using No. 1 Implemented Example. In the following, the process is explained starting from Fig. 2A and in order.

First of all, in Fig. 2A, the Au layer (12) of thickness 1 [μ], Ni layer (13) of thickness 1 [μ], and Au layer (14) of thickness 3 [μ] are plated on top of the substrate (11) of Fe in order, and installed the chip connection part (16) and external electrode parts (17) (18), which are consisting of the chip (15) for the semiconductor equipment, onto the specific locations of the chip connection

part (11g) and external electrode connection parts (11h) (11i) on the above-mentioned substrate (11), respectively.

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In Fig. 3, the plan view of the above-mentioned substrate (11), on which the process that is shown in Fig. 2A has been completed, is shown. Next, in Fig. 2B, after having installed the chip (15) onto the above-mentioned chip connection part (16), connect the chip (15) and above-mentioned external electrode parts (17) (18) with the wire (19), which are composed of Au small wires, respectively, by means of the wire bonding method. Next, in Fig. 2C, in order to integrate the above-mentioned external electrode parts (17) (18), which are being installed on the substrate (11) that is shown in Fig. 2B, chip connection part (16), chip (15), and wire (19), establish the resin molding layer (20), which is composed of an epoxy, onto the above-mentioned substrate (11) by means of the well-known transfer-molding method. In this implemented example, the thickness "t" of the above-mentioned resin molding layer (20) has been set to 1 [mm].

Next, in Fig. 2C, only the Fe is etched selectively, however, the resin molding layer (20) and Au layer (12) are not etched practically by spray-etching from the back side (11a) of substrate (11) with such a solution like a ferric chloride (FeCl_3) for example, by which the etching can be avoided, so that the above-mentioned substrate (11) is removed, and that the lead-less type packaging (21) that is shown in Fig. 2D can be completed. Among the bottom surfaces of the Au layer (12), which were exposed by the previous etching, the external electrode parts (17) (18) at the bottom surface of the Au layer (12) turn out to be the external electrode surfaces (12b) (12c), and the bottom surface of the Au layer (12) at the chip connection part (16) turns out to be the

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heat dissipation surface (12a).

When installing the packaging (21), which was completed throughout the above-mentioned process, onto the printed substrate, the above-mentioned external electrode surfaces (12b) (12c) that are shown in Fig. 2D can be connected directly to the conductor patterns on the printed substrate by soldering.

The above-mentioned heat dissipation surface (12a) in No. 1 Implemented Example turns out to be a heat dissipation surface for the heat that is generated by the chip (15) while it is working. Since the heat conductivity of a metal is extremely high, the heat that is generated by the chip (15) flows very quickly towards outside alongside the chip connection part (16), which is made of a metal, and removed effectively through the heat dissipation surface (12a). However, in order to remove the heat that is generated by the chip (15) more effectively, it is desirable that a part of the heat dissipation fins, which all together possess a broad surface area, is pushed to the above-mentioned heat dissipation surface (12a), so that the heat is removed through air cooling.

Since the packaging (21), which is explained in No. 1 Implemented Example, can be produced by such a simple process that is shown in Fig. 2A ~ 2D, the equipment which is being used for the conventional method can be utilized throughout the entire process. Not only that, those special equipment which was mentioned previously and required for producing the chip-carrier type packaging is needed at here. Therefore, it is possible that to produce the lead-less type packaging (21) for semiconductor equipment, which has a high heat dissipation capacity as well as with more reliable capabilities, through an automated, simple, and less expensive ways. Moreover, in the above-mentioned No. Implemented Example, the transfer-molding method is employed as the method of forming the resin molding layer (20). This transfer-molding method will provide such an advantage that not only producing a reliable resin molding material, but also makes it possible

to produce the packaging in an automated manner, based on its easy molding automation and mass-production features.

In the above-mentioned No. 1 Implemented Example, just like the case that is shown in Fig. 2A, by slightly etching the upper surface of the substrate (11) with the previously mentioned FeCl_3 solution after having installed the chip connection part (16) and external electrode parts (17) (18), the undercut parts (11a) ~ (11f) can be formed on the substrate (11), which is under the chip connection part (16) and external electrode parts (17) (18), as shown in Fig. 4A, and the packaging (21) that is shown in Fig. 4B can be completed in the same method as shown in Fig. 2B ~ 2D. In this way, since the above-mentioned undercut parts (11a) ~ (11f) can be formed at the bottom of the chip connection part (16) and external electrode parts (17) (18) by means of the etching, which was described previously, the protruded parts (20a) ~ (20f) can be formed with the resins filling up the parts. Therefore, the above-mentioned chip connection part (16) and external electrode parts (17) (18) are supported by these protruded parts (20a) ~ (20f) from the bottom subsequently, and that the chip connection part (16) and external electrode parts (17) (18) can be prevented from falling off from the resin-molding layer (20) while the packaging (21) is used.

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Moreover, as the chip connection part (16) and external electrode parts (17) (18) are formed in such a way that not being protruded from the bottom surface of the resin molding layer (20), both of these chip connection part (16) and external electrode parts (17) (18) can be protected further.

Fig. 5A ~ 5C are showing the process diagrams to explain the production method of packaging for semiconductor equipment, which is related to this invention by using No. 2 Implemented Example. In the following, the process is explained starting from Fig. 5A and in order.

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First of all, in Fig. 5A, after having sprayed the well-known photo-resist on to the top surface of the substrate (11), which is 35 [μ] thick and made of Cu, execute the specific patterning. Next, by using such a solution like a ferric chloride (FeCl_3) that is previously mentioned for example, and by which only the Cu can be selectively etched, the surface of the above-mentioned substrate (11) is slightly etched, so that the chip connecting part (11g) and external electrode connecting parts (11h) (11i) can be formed individually on the surface of the above-mentioned substrate (11). And, after having removed the above-mentioned photo-resist, connect the chip (15) to the above-mentioned chip connecting part (11g) through the soldering layer (23), just as it was done in Fig. 5B for No.1 Implemented Example, and connect the chip (15) and above-mentioned external electrode parts (11h) (11i) with the wire (19), which are composed of Au small wires, respectively, by means of the wire bonding method. In this implemented example, however, a larger diameter of wire than the one that was used for No. 1 Implemented Example was used, due to the reasons that would be explained later in this report. Next, establish the resin molding layer (20) on the above-mentioned substrate (11), just as the same way that was done for No. 1 Implemented Example. And, next complete the packaging (24) by removing the etching on the above-mentioned substrate (11), just as the same way that was done for No. 1 Implemented Example. The end part of wire (19), which was exposed by the previous etching turns out to be the external electrode parts (17) (18), and the bottom surface of the soldering layer (24) turns out to be the heat dissipation surface (23a).

When installing the packaging (24), which was completed throughout the above-mentioned process, onto the printed substrate, the above-mentioned external electrode parts (17) (18) that are shown in Fig. 5D can be connected directly to the conductor patterns on the printed substrate by soldering, the same way that was used for No. 1 Implemented Example. As it is clear now by

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the above reasons, since the ends of the wire (19) are used as the external electrode parts (17) (18) in this implemented example, it is desirable to use the larger diameter of wire (19) as it was mentioned previously. The function of the heat dissipation surface (23a) is the same as it was for No. 1 Implemented Example.

The packaging (24) for the above-mentioned No. 2 Implemented Example is a little different from the packaging (21) for No. 1 Implemented Example, and the external electrode connection parts (11h) (11i), which were installed during the photo-resist and etching processes, are being connected directly to the wire (19), thus requiring no formations of the Au layer (12)(14) and Ni layer (13) that had been established for the packaging of No. 1 Implemented Example. The photo-resist and etching processes for the above case is much simpler compared with the plating process that was used for the packaging (21) for No. 1 Implemented Example. Also, by implementing this photo-resist and etching processes, the usage of such a precious metal like Au is going to be eliminated.

In the above-mentioned No. 1 and No. 2 Implemented Examples, it was mentioned with regard to a single chip to be installed at the single chip connection part and resin molding. However, based on this prototype idea, it is also possible to produce multiple numbers of packaging, all of which will have a single chip individually, at the same time, by installing multiple numbers of chip connection parts on a substrate, attaching multiple numbers of chips individually, resin molding in an integrated manner, and finally cut into the pieces. Furthermore, after having installed various kinds of chips and passive devices such as, condenser and resistors onto the substrate, and resin molding integrally, it is possible to produce the packaging that will have a various kind of functions, as well as the ones with highly integrated circuit element.

As the materials for the substrate for the above-mentioned No. 1 Implemented Example, it may

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be another type of metal, such as Cu and the like, as long as the selective etching is possible, and by the same token, the materials for the substrate for the above-mentioned No. 2 Implemented Example, it may be some other type of metal, such as Fe and the like. Moreover, in the case of No. 1 Implemented Example, some other type of materials such as, polyimide type resin can be used as well. In this case,

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however, a mixture of hydrazine and ethylenediamine can be used as the etching liquid that was mentioned previously.

Effect of the Invention:

By the production method of packaging for semiconductor equipment, which is related to this invention, it is possible to produce the small size of packaging, which has a high heat dissipation capacity for the heat that is generated by the semiconductor equipment at the time of operation, as well as with more reliable capabilities, through an automated, relatively simple, and less expensive way.

4. Brief Descriptions for Sketched Diagrams

Fig. 1 shows the sectional view of chip-carrier type packaging construction of the conventional plastic type, and Fig. 2A ~ 2D are showing the process diagrams to explain the production method of packaging for semiconductor equipment, which is related to this invention by using No. 1 Implemented Example. Fig. 3 shows the plan view of substrate on which the process that is shown in Fig. 2A has been completed, and Fig. 4A and 4E are showing the similar views as the previous Fig. 2A ~ 2D, which are showing the deformed example of above-mentioned No. 1 Implemented Example. Fig. 5A ~ 5C are showing the process diagrams to explain the production

method of packaging for semiconductor equipment, which is related to this invention by using
No. 2 Implemented Example.

And, in these diagrams, the following Item Numbers are representing;

(1), (21), (22), and (24) ----- Packaging
(2), and (15) ----- Chip
(3), and (19) ----- Wire
(11) ----- Substrate
(11h), and (11i) ----- External Electrode Connection Parts
(17), and (18) ----- External Electrode Part
(20) ----- Resin Molding Layer

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Fig. 1

Fig. 2A

Fig. 2B

Fig. 2C

Fig. 2D

Fig. 3

Fig. 4A

Fig. 4B

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Fig. 5A

Fig. 5B

Fig. 5C

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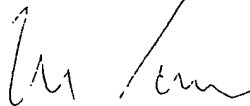
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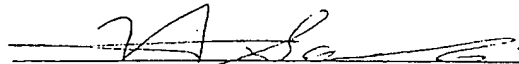
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⑭ 半導体装置のパッケージの製造方法

35号ソニー株式会社内

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明 細 書

1. 発明の名称

半導体装置のパッケージの製造方法

2. 特許請求の範囲

選択エンタング可能な材料から成る基板上に半導体装置を配置し、接続用ワイヤを上記半導体装置に接続すると共にこの接続用ワイヤの外部電極部を上記基板の外部電極形成部位に接続し、次いで上記基板上において上記半導体装置及び上記接続用ワイヤを一体に樹脂セーンドし、しかる後上記基板をエンタング除去することを特徴とする半導体装置のパッケージの製造方法。

3. 発明の詳細な説明

従来の利用分野

本発明は、半導体装置のパッケージの製造方法に関する。

4. 技術とその問題点

従来、プリント基板上の実装位置の低いパッケージとして、チップキャリアタイプのパッケージが知られている。このパッケージはリードレス

タイプのパッケージで、パッケージの底面に引き出されているハンダ付け可能な直線をプリント基板の導体パッドに直接ハンダ付けして接続することにより実装を行うものである。

このチップキャリアタイプパッケージには、セパミンクタイプとブラセナクタイプとがある。セパミンクタイプはパッケージ自体が絶縁体であるばかりでなく、プリント基板に直接ハンダ付けすると、加熱サイクル時にセパミンク^スと上記ハンダ及び上記導体との間の熱膨張係数の差によつて接続部には割れやクラックが生じる恐れがあるという欠点を有している。一方、ブラセナクタイプはパッケージが金属であるという利点を有しているが、熱膨張係数が多く、また形状がパッケージの製造の自動化に適していないという欠点を有している。

このような従来のブラセナクタイプのチップキャリアタイプパッケージの構造を第1図に示す。このパッケージ(1)は、銅箔製の基板(2)が平面的形成されているプリント基板(3)上に半導体装置を構成

するチップ(4)を搬出し、ワイヤボンディング法により上記チップ(4)と上記電極(2)の一端とをAuの糊から成るワイヤ(5)で接続した後、上より板状のエポキシ樹脂を滴下させて硬化反応することにより作成する。

このパッケージ(1)において、チップ(4)は樹脂層(6)とプリント基板(3)とによつて囲まれている。これらの樹脂層(6)及びプリント基板(3)の熱抵抗は共に大きいので、その動作時においてチップ(4)で発生する熱をパッケージ(1)の外側に効果的に放散することができない。即ち、このパッケージ(1)は放散性が低いという欠点を有している。また上記の板状のエポキシ樹脂を滴下する際に、滴下の樹脂を一定量、しかも高速度で滴下することが難しく、このためにパッケージ(1)はパッケージの製造の自動化に適していないという欠点を有している。

一方、上述のチップキャリアタイプパッケージとは異なるパッケージにテープキャリアタイプパッケージがある。このタイプのパッケージは従来のチップキャリアタイプパッケージよりもさらに

小型化できるという利点を有するが、チップが樹脂層によつて完全に覆われているため熱放散性が良好でないこと、テープを用いているために特殊な装置が必要である等の欠点を有している。

発明の目的

本発明は、上述の問題にかんがみ、熱放散性が良好かつ信頼性の高い半導体装置のパッケージの製造方法を提供することを目的とする。

発明の概要

本発明に係る半導体装置のパッケージの製造方法は、選択エッチング可能な材料から成る基板上に半導体装置を搬出し、接続用ワイヤを上記半導体装置に接続すると共にこの接続用ワイヤの外部電極部を上記基板の外部電極接続部位に接続し、次いで上記基板上において上記半導体装置及び上記接続用ワイヤを一体に封入モードし、しかる後上記基板をエッチング除去するようにしている。このようにすることによつて、熱放散性が良好かつ信頼性の高いリードレスタイプのパッケージを、簡便かつ安価な方法によつて自動的に製造す

ることができる。なお上記外部電極部は上記接続用ワイヤ自体が兼ねていてもよいし、上記接続用ワイヤとは別に設けられかつ上記接続用ワイヤが接続されているものでもよい。

実施例

以下本発明に係る半導体装置のパッケージの製造方法の実例につき図面を参照しながら説明する。

第2A図～第2D図は本発明の第1実施例による半導体装置のパッケージの製造方法を説明するための工程図である。以下第2A図から工程図を説明する。

まず第2A図において、厚さ $5(\mu)$ のFe板の基板(1a)上に、厚さ $1(\mu)$ のAu層(2a)、厚さ $1(\mu)$ のNi層(2b)及び厚さ $3(\mu)$ のAu層(2c)を形成し、半導体装置を形成するチップ(4)の表面電極及び外部電極部(2d)のそれぞれを上記基板(1a)の所定のチップ載置部位(11a)及び外部電極接続部位(11b)(11c)のそれぞれに設ける。第2A図に示す工程終了後の上記基板(1a)の平面図を示

す図に示す。次に第2B図において、上記チップ載置部位(11a)にチップ(4)を搬出した後、ワイヤボンディング法によつてこのチップ(4)と上記外部電極部(2d)とをそれぞれAuの糊から成るワイヤ(5)で接続する。次に第2C図において、第2B図の基板(1a)の上に設けられた上記外部電極部(2d)、チップ(4)及びワイヤ(5)を一体とするために、公知のトランスファ・モード法(移送反応)を用いて、エポキシから成る樹脂モード樹脂を上記基板(1a)上に形成する。なお本実施例においては、上記樹脂モード樹脂の厚さ t を $1(\mu)$ とした。

次に第2D図において、Feのみを選択的にエッチングするが樹脂モード樹脂及びAu層(2a)はエッチングしないエッチング液、例えば酸化第二鉄($FeCl_2$)溶液を用いて、基板(1a)の表面(11a)側からスプレーエッチングすることにより、上記基板(1a)を除去して、第2D図に示すリードレスタイプのパッケージ(1)を完成させる。上記エッチングによつて露出されたAu層(2c)の下面のうち外部

電極部104のAu層105の下面が外部電極面(12b)(12c)となり、またチップ設置部104のAu層105の下面が熱放散面(12a)となる。

上述のようにして完成されたパッケージ100をプリント基板上に実装する場合に、第2D図に示す上記外部電極面(12b)(12c)をプリント基板上の導体パターンに低抵抗ハンダ付けして接続すればよい。

上述の第1実施例の熱放散面(12a)は、その動作時においてチップ104から発生する熱の放散面となつてゐる。金属の熱伝導率は非常に高いので、チップ104から発生する熱は金属製のチップ設置部104を外方に向かつて迅速に伝れて、熱放散面(12a)から放散されることによつて効果的に除去される。しかし、より効果的にチップ104の発生熱を除去するためには、広い表面積を有する放熱フィンの一部を上記熱放散面(12a)に押し当てて空介により熱を放散させるのが好ましい。

上述の第1実施例のパッケージ100は第2A図～第2D図に示すような簡単な工程によつて作るこ

とができるばかりでなく、全ての製造工程に従来から用いられている装置を用いることができるので、テープキャリアタイプのパッケージにおいて必要な特殊な装置が不要である。従つて、簡便かつ安価な方法によりパッケージ100を製造することができる。さらに上述の第1実施例では樹脂モールド層106を形成する方法としてトランスファ・モールド法(移送成形法)を用いている。この方法は信頼性の高い樹脂封止ができるばかりでなく、モールドの微細化、重産化が容易であるためにパッケージを自動的に製造できるという利点を有している。

なお上述の第1実施例において、第2A図に示す基板と同様にチップ設置部104及び外部電極部104を設けた後に、基板101の上面を前述のFeCl₃溶液を用いて僅かにエッチングすることにより、第4A図に示すようにチップ設置部104及び外部電極部104の下部の基板101にアンダーコート部(11a)～(11f)を形成し、次に第2B図～第2D図と同様な方法によつて第4B図に示すパッケージ100を

完成させることができる。このように上記のエッチングによつてチップ設置部104及び外部電極部104の下部に上記アンダーコート部(11a)～(11f)が形成されるので、これらの部分に樹脂が回り込んで突出部(20a)～(20f)が形成される。従つてこれらの突出部(20a)～(20f)によつて上記チップ設置部104及び上記外部電極部104が下方から保護される状態となるので、上記チップ設置部104及び上記外部電極部104が樹脂モールド層106の下面から突出することなく形成されるので、これらのチップ設置部104及び外部電極部104を保護することができるという利点もある。

第5A図～第5C図は本発明の第2実施例による半体封装のパッケージの製造方法を説明するための工程図である。以下第5A図から工程順に説明する。

まず第5A図において、厚さ5μm程度のCu

製の基板101の上面に公知のフォトリソストを塗布した後に所定のパターンニングを行う。次にCuのみを選択的にエッチングするエッチングは、例えば前述のFeCl₃溶液を用いて上記基板101の表面を僅かにエッチングすることによつて、上記基板101の表面にチップ設置部104及び外部電極部104(11b)(11i)をそれぞれ形成する。上記フォトリソストを除去した後に第5B図において、第1実施例と同様に、上記チップ設置部104(11g)にハンダ層106を介してチップ104を取付した後、ワイヤボンディング法によつてこのチップ104と上記外部電極部104(11h)(11i)とをそれぞれAuの細線から成るワイヤ107で接続する。なお本実施例においては、前述の理由により、第1実施例で用いたワイヤよりも径の大きいワイヤを用いた。次に第1実施例と同様に樹脂モールド層106を上記基板101上に形成する。次に上記基板101を第1実施例と同様な方法でエッチング除去してパッケージ100を完成させる。上記エッチングにより露出されたワイヤ107の露部が外部電極部104となり、またハ

ンダ積層の下画が被放線部(23a)となる。

上画のようにして完成されたパッケージ部をプリント基板上に実装する場合には、第1実施例と同様に、図5C図に示す上記外部電極部部材をプリント基板上の母体パターンに直接ハンダ付けして接続すればよい。このことから明かなように、本実施例においてはワイヤ時の塗部をそのまま外部電極部部材として用いるために、ワイヤ時の塗を前述のように大きくするのが好ましい。なお被放線部(23a)の接続は第1実施例と同様である。

上述の第2実施例のパッケージ部は、第1実施例のパッケージ部と異なり、フォトリソ工法及びエッチング工法によつて形成時に設けられた外部電極被放線部(11a)(11b)にワイヤ部を直接接続するようにしているため、第1実施例のパッケージ部におけるAu層部及びNi層部を形成する必要がない。上記のフォトリソ工法及びエッチング工法は第1実施例のパッケージ部で用いたメッキ工法よりもさらに簡便である。またこれらのフォトリソ工法及びエッチング工法

を用いることにより、Au等の貴金属を用いる必要がなくなるという利点がある。

上述の第1実施例及び第2実施例においては、1個のチップをチップ駆動部に接続してこれを同相モードする場合につき述べたが、並列に多数のチップ駆動部を取り、それぞれのチップ駆動部に同一のチップを接続して、これらのチップを一体に同相モードした後に切断分離することにより、それぞれ1個のチップを有する同一のパッケージを多数個同時に作ることもできる。また複数のチップと、コンデンサや抵抗等の受動素子とを基板上に接続した後これらを一体に同相モードすれば、種々の機能を有するパッケージを作ることができると共に、回路素子の集積度の高いパッケージを作ることができるといふ利点がある。

上述の第1実施例の基板の材料は選択エッチングが可能であればCu等の他の金属であつてもよく、また第2実施例の基板の材料もFe等の他の金属であつてもよい。第1実施例においてはさらに金属以外の材料、例えばポリイミドやエポキシ

樹脂を用いることも可能である。この場合には前述のエッチング液としては、ヒドラジンとエタレンジアミンとの混合液を用いればよい。

説明の符号

本発明に係る半導体装置のパッケージの製造方法によれば、その動作時において半導体表面から発生する熱の放散性が良好でありかつ信頼性が高い小型のパッケージを、極めて簡便かつ安価な方法によつて自動的に製造することができるといふ利点がある。

4 図面の簡単な説明

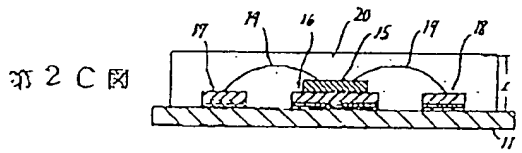
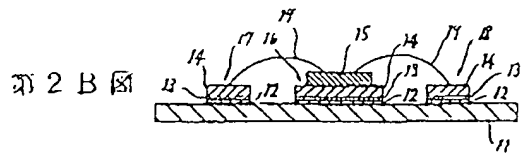
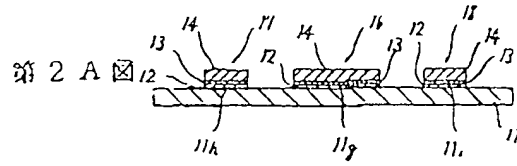
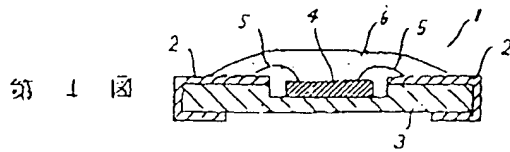
図1図は従来のブラスタックタイプのチップキャリアタイプパッケージの構造を示す断面図、図2A図～図2D図は本発明の第1実施例による半導体装置のパッケージの製造方法を説明するための工程図、図3図は上記図2A図に示す工程終了後の状態の断面図、図4A図及び図4B図は上記図1図の被放線部を示す上記図2A図～図2D図と同様の図、図5A図～図5C図は本発明の第2実施例による半導体装置のパッケージの製造方法を説明するための工程図である。

なお図面に附いた符号において、

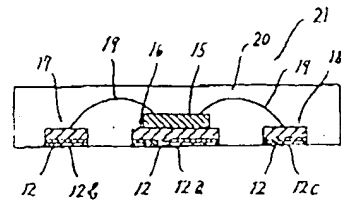
(12)(13)(14)	パッケージ
(15)	チップ
(16)	ワイヤ
(17)	被放線部
(18a)(18b)	外部電極被放線部
(19)	外部電極部
(20)	同相モード部

である。

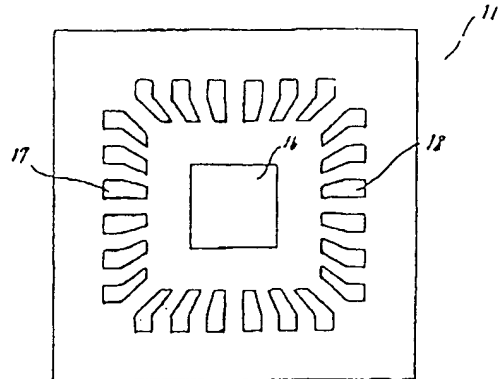
代	述	人	士	氏	勝
、					名
、					姓



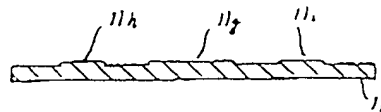
第 2 D 圖



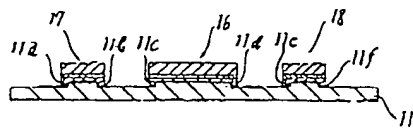
第 3 圖



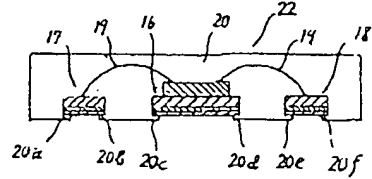
第 5 A 圖



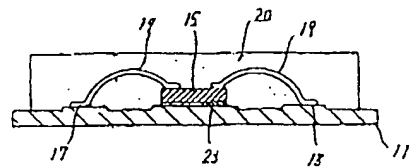
第 4 A 圖



第 4 B 圖



第 5 B 圖



第 5 C 圖

